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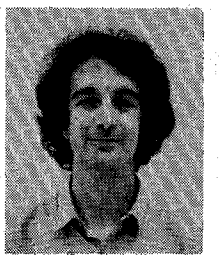

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Backgating in GaAs MESFET's

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Abstract—**The phenomenon of backgating in GaAs depletion mode MESFET devices is investigated. The origin of this effect is electron trapping on the Cr^{2+} and EL(2) levels at the semi-insulating substrate-channel region interface. A model describing backgating, based on DLTS and spectral measurements, is presented. Calculations based on this model predict that closely compensated substrate material will minimize backgating. Preliminary experimental data support this prediction.**

I. Introduction

THE characteristics of GaAs metal-semiconductor field effect transistors (MESFET's) depend strongly on the properties of the interface between the *n*-type active region and the semi-insulating substrate [1]. GaAs MESFET's can exhibit phenomena such as a drift in the drain current with time and a change in the drain current as a result of a change in the substrate bias. The decrease in the drain current when a negative voltage is applied to the substrate is termed backgating [2], [3]. Backgating is a detrimental effect in complex GaAs integrated circuits due to the interaction between closely spaced devices. This effect is caused by the relatively large capacitance of the substrate-active channel interface due to negative charge accumulated on deep traps in the interface region. The application of a bias to the substrate modulates this space charge region. This results in a change in the active channel region width and, therefore, a change in the drain current. In this paper, we will present the results of investigations into the physical nature of the deep traps responsible for backgating. Based on these investigations, we propose a model which explains backgating and demonstrate one solution, namely the use of closely compensated substrate material to minimize the back-side channel capacitance.

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II. Experimental Procedure

A. Substrate Material

GaAs MESFET's fabricated in four different types of substrate materials were investigated. The active region for the devices is produced by ion implantation into: 1) Cr-doped semi-insulating substrates (with Cr concentrations between 5×10^{15} and 1×10^{17} cm^{-3}); 2) high purity semi-insulating substrates (grown with no intentionally added dopants); 3) buffer layers on Cr-doped substrates; and 4) buffer layers on high purity substrates.

The substrate material, both Cr-doped and high purity, is grown by the two-atmosphere liquid encapsulated Czochralski (LEC) technique [4]. Chromium incorporates into the GaAs lattice on Ga sites and gives up three electrons to the bonds. The neutral state of Cr with respect to the lattice is Cr^{3+} with the electron configuration $3d^3$. Capture of electrons leads successively to the core states $3d^4$, Cr^{2+} (a singly, negatively charged acceptor), and $3d^5$, Cr^{1+} (a doubly, negatively charged acceptor). Chromium which is neutral, Cr^{3+}, is a double acceptor. The Cr^{2+} and Cr^{3+} levels are located 0.70 eV [5] and 0.45 eV [6] above the valence band, respectively, as shown in the energy level diagram of Fig. 1. There is uncertainty concerning the position of the Cr^{4+} and Cr^{1+} levels. According to the literature, the Cr^{4+} level is 0.15 eV [6] above the valence band and the Cr^{1+} level is degenerate with the conduction

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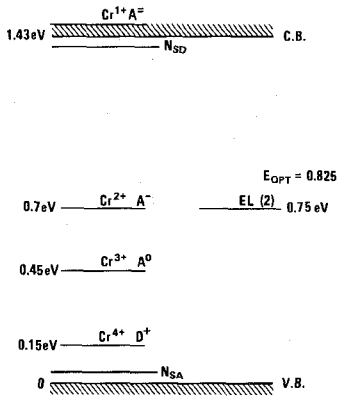

Fig. 1. Energy level diagram of Cr-doped GaAs.

band [7]. The Cr^{2+} and Cr^{3+} levels are the most important to the understanding of the behavior of Cr-doped semi-insulating GaAs.

The other commonly observed level in GaAs is the EL(2) donor level which is responsible for the high resistivity of nonintentionally doped, high-purity GaAs [8]. This level is believed to be due to an anti-site defect, Ga on an As site [9]. It is located 0.75 eV below the conduction band (thermal activation energy); the optical ionization energy is 0.82 eV [10]. The necessary conditions for the production of high-resistivity material is that the dopants satisfy the following relations:

$$\text{if } N_d > N_a \text{ then } (N_{da} - N_{dd}) > (N_d - N_a), \text{ [11]} \quad (1)$$

or

$$\text{if } N_a > N_d \text{ then } (N_{dd} - N_{da}) > (N_a - N_d), \text{ [12]} \quad (2)$$

where N_d and N_a are the concentrations of shallow donors and acceptors, respectively, and N_{dd} and N_{da} are the concentrations of deep donors, EL(2), and acceptors, Cr, respectively. The recent paper by Martin describes the compensation mechanisms in detail [13].

The high-purity buffer layers are grown on the Cr-doped or high-purity semi-insulating substrates by the liquid-phase epitaxy (LPE) technique. These layers are grown in a horizontal graphite slider system at 700°C. This epitaxial material, characterized using Hall measurements, is n-type with mobilities measured at room temperature of approximately 8000 $cm^2\ V^{-1}\ s^{-1}$ and mobilities measured at 77 K are greater than 120 000 $cm^2\ V^{-1}\ s^{-1}$. The measured free-carrier concentration at room temperature is less than $1\times10^{14}\ cm^{-3}$ [14]. The buffer layers used in this investigation are approximately 3 μm thick and are fully depleted by the surface and semi-insulator to buffer layer interface space charge regions.

The depletion mode MESFET test devices, shown in Fig. 2, are fabricated using selective region ion implantation. The MESFET channel regions are formed by localized ion implantation of 500-keV Se ions to a dose of 6×10^{12} cm^{-2}. A second localized Si implant at 500 keV to a dose of $1\times10^{13}\ cm^{-2}$ is used in the ohmic contact regions to lower the sheet resistance. The implants are simultaneously annealed at 850°C for 15 min using a Si_3N_4 cap. The

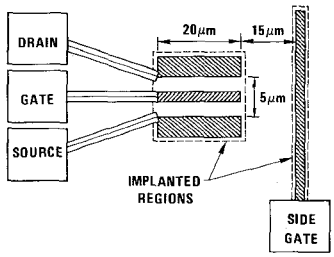

Fig. 2. The MESFET test structure used in the backgating, DLTS, and spectral response experiments.

MESFET fabrication includes a recessed gate technology which reduces the modulation of the drain current due to changing depletion layer widths at the free surface during switching transients and also allows the adjustment of the gate cutoff voltage during the device processing [15]. The side-gate electrode is an ohmic contact to an implanted region. This region is isolated from the active region of the MESFET by the semi-insulating substrate or the fully depleted buffer layer.

III. Experimental Results

The magnitude of the backgating effect is determined by measuring the change in the saturated drain current as a result of the application of a negative voltage to the side-gate electrode. In these experiments, the source–drain bias is 4 V, the gate is shorted to the source, and the side-gate bias is −4 V. Results obtained from these devices fabricated in wafers of the types listed above are presented in Fig. 3. These data represent the mean and one sigma variation of the drain-current change with the application of −4-V side-gate voltage for approximately 30 devices on a one-inch-square wafer. These data illustrate the wide spread in the magnitude of backgating on a single wafer and the large variation of the effect from wafer to wafer. In general, the effect is less for buffer layers on Cr-doped substrates than for high-purity substrates, with or without a buffer. The buffer layers used in this experiment had little influence on backgating. This is not understood since the buffer layer should decrease the capacitance between the substrate and the active layer and therefore decrease the magnitude of backgating. Experiments to investigate the effect of buffer layers are in progress. The sample on the Cr-doped substrate was fabricated in closely compensated material. This will be discussed in detail later.

The time dependence of the drain current following the application of a side-gate potential is shown in Fig. 4. There is a rapid decrease in current when the side-gate bias is applied followed by an additional slow decrease for Cr-doped substrates and a slow increase for high-purity substrates. The general form of the drain-current transients for buffer layers on the different types of substrates is the same as observed without the buffer layer. The magnitude of the drain-current change depends on the particular substrate as illustrated in Fig. 3. These current transients can be understood by considering the band diagram shown in Fig. 5. Negative charge is accumulated on deep levels on the substrate side of the substrate-channel region interface.

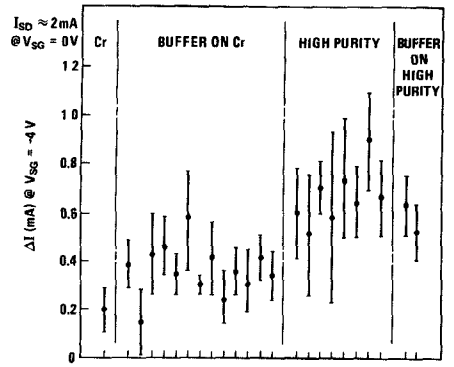

Fig. 3. Backgating results measured on devices fabricated in different substrate materials.

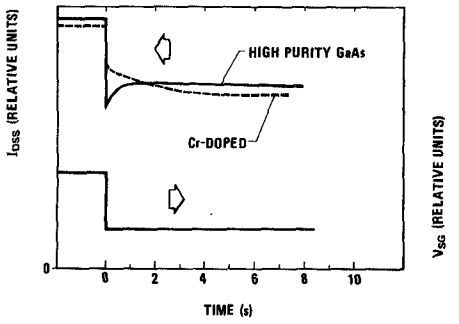

Fig. 4. Typical time dependence of the drain current for Cr-doped and high-purity substrates after the application of a side-gate voltage.

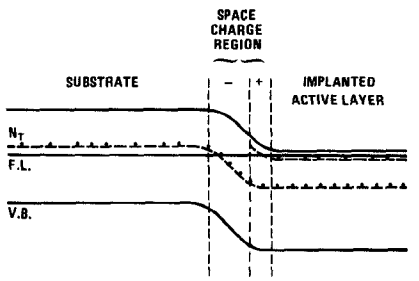

Fig. 5. The energy band diagram of the substrate-active region interface.

This negative charge is balanced by the positive space charge region in the channel region and produces the relatively large capacitance of the substrate-channel region interface. A negative potential applied to the substrate increases the width of the depletion region at the back side of the MESFET channel which results in the rapid decrease of the drain current. This change in the depletion layer width is followed by the emission of electrons or holes from the deep levels as equilibrium is reestablished. In the case of Cr-doped substrates, holes are emitted from the deep Cr level which results in a further decrease in the drain current because of the increase of the negative charge on the substrate side of the interface. In the high-purity substrates, electrons are emitted to the conduction band from the EL(2) level and the drain current increases to an equilibrium value.

These drain-current transients have been analyzed using an automated conductance DLTS system [16]. In this technique, the transients are analyzed at a number of temperatures to derive the activation energies and the capture cross sections of the levels responsible for the change in the drain current following the application of the side-gate voltage. The results obtained by this technique for Cr-doped and high-purity substrates are summarized in Table I. In Cr-doped substrates, the major DLTS peak is due to the emission of holes from the Cr level to the valence band. The major DLTS peak in high-purity substrates is due to the emission of electrons from the EL(2) level to the conduction band. The activation energies and the capture cross sections determined in this investigation agree with those reported by Martin [17].

TABLE I
DEEP LEVELS DETERMINED BY DLTS MEASUREMENTS OF THE BACKGATING TRANSIENTS

Cr-DOPED			HIGH-PURITY		
LEVEL	ACTIVATION ENERGY (eV)	CAPTURE CROSS-SECTION (cm^2)	LEVEL	ACTIVATION ENERGY (eV)	CAPTURE CROSS-SECTION (cm^2)
Cr	0.781	7e − 15	EL (2)	0.82	2.7e − 13
HL	0.644	1.1e − 13	EL	0.692	2.0e − 13
HL	0.516	1.4e − 13	HL	0.535	4.1e − 15

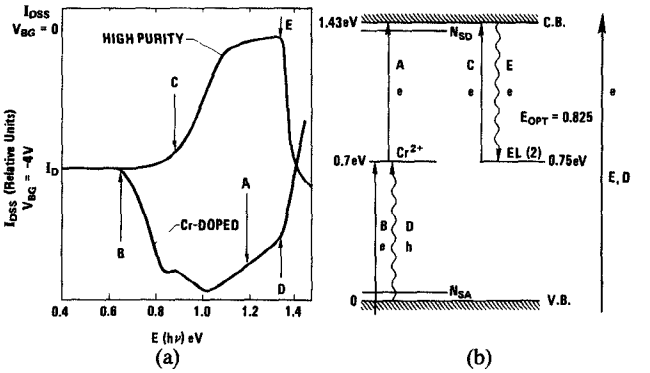

Fig. 6. (a) Spectral dependence of backgating for Cr-doped and high-purity substrates. (b) Energy level diagram showing the transitions responsible for the spectral response.

The spectral dependence of backgating has been measured to obtain additional information regarding the levels responsible for the effect and to understand ambient light effects on the MESFET characteristics. Typical spectral dependence of the changes in the saturated drain current, measured with a side-gate voltage of −4 V, for Cr-doped and high-purity substrates are shown in Fig. 6(a). The transitions responsible for the spectral dependence of the drain current are indicated on the energy level diagram of Fig. 6(b). In the case of the Cr-doped substrates, the decrease of the current in the range of 0.65 eV to 1.0 eV is caused by the increase of backgating due to electron transitions from the valence band to the Cr^{3+} level. These transitions produce chromium in the Cr^{2+} charge state. The holes created in the valence band by this transition are swept away by the electric field in the space charge region at the substrate-channel region interface. This increase in the charge on the Cr^{2+} level increases depletion depth into

the MESFET channel, as indicated in Fig. 5, and therefore the drain current decreases. The increase of the current at 1.0 eV is caused by electron transitions from the Cr^{2+} level to the conduction band which reduces the negative charge in the junction, decreases the depletion width, and increases the drain current. Since the Cr^{2+} level is close to the center of the band gap both transitions, valence band to the Cr^{2+} level and Cr^{2+} level to the conduction band, are possible. In the photon energy range from 0.65 eV to 1.0 eV, the optical cross section for electron transitions from the valence band to the Cr level σ_p^0 is greater than the optical cross section for electron transitions from the Cr level to the conduction band σ_n^0, and therefore the transition producing electrons in the Cr^{2+} state is dominant. In the range from 1.0 eV to 1.4 eV, $\sigma_n^0 > \sigma_n^0$, and therefore the transition of electrons from the Cr^{2+} level to the conduction band is dominant [10]. A steep increase in current is seen at the band-gap photon energy because electron-hole pairs are generated and the holes are trapped by the Cr^{2+} level while the electrons are swept away by the space charge field. This results in a decrease in the negative charge at the interface and an increase in the current.

The spectral dependence of backgating is quite different in the case of high-purity substrates. An increase of the drain current is observed with a threshold of 0.8 eV which agrees with the optical ionization energy of the EL(2) deep level [10]. These transitions decrease the concentration of the negative charge on the substrate side of the interface which produces a wider channel region and the increase in the drain current. The drain current decreases as the photon energy approaches the band-gap energy. In this region, electron-hole pairs are generated and the electrons are captured by the EL(2) level. This increase in the negative charge reduces the drain current as discussed above. It should be noted that there is almost no backgating effect when the high-purity substrate is illuminated with 1.2-eV light. In this condition, no change in the drain current is seen when a side-gate potential is applied.

IV. Backgating Model

A model which is consistent with the experimental results obtained on structures without buffer layers is postulated. The experiments described above indicate that backgating in Cr-doped substrates is caused by the accumulation of negative charge on the Cr^{2+} level (fast transient) and by the emission of holes from the Cr level (slow transient). For high-purity substrates, backgating is caused by the accumulation of negative charge on the EL(2) level (fast transient) and by the emission of electrons from the EL(2) level (slow transient). The net concentration of negative charge, at equilibrium, on the substrate side of the substrate-channel region interface N_{eff} depends on the occupancy of the deep traps in the bulk according to the following relationship:

$$N_{\text{eff}} = N_{\text{Cr}}\left\{e_p^{\text{Cr}}/\left(e_p^{\text{Cr}}+e_n^{\text{Cr}}\right) - 1/\left[1+\exp\left[\left(E_{Cr^{2+}}-E_f\right)/kT\right]\right]\right\} + N_{\text{EL(2)}}\left\{e_p^{\text{EL(2)}}/\left[e_p^{\text{EL(2)}}+e_n^{\text{EL(2)}}\right] - 1/\left[1+\exp\left[\left(E_{\text{EL(2)}}-E_f\right)/kT\right]\right]\right\} \quad (3)$$

where

N_{Cr}	total chromium concentration in the substrate,
$N_{\text{EL(2)}}$	total EL(2) level concentration in the substrate,
e_p^{Cr}	emission rate for holes from the Cr^{3+} level,
e_n^{Cr}	emission rate for electrons from the Cr^{2+} level,
$e_p^{\text{EL(2)}}$ and $e_n^{\text{EL(2)}}$	emission rates for holes and electrons from the EL(2) level, respectively,
$E_{Cr^{2+}}$ and $E_{\text{EL(2)}}$	thermal activation energies with respect to the valence band for the Cr^{2+} and EL(2) levels, respectively, and
E_f	energy of the Fermi level with respect to the valence band in the bulk of the substrate.

In this equation, the Fermi-function terms give the concentration of negative charge on the deep levels in the bulk. The emission-rate terms give the concentration of negative charge in the space charge region. The emission rates are derived from the capture cross sections given in the literature [17]. The difference between the emission-rate terms and the Fermi-function terms is the excess concentration of negative charge on the deep levels on the substrate side of the substrate-channel region interface.

Since the relative occupancy of the deep levels in the space charge region is fixed by the appropriate emission rates, the concentration of negative charge at the interface is controlled by the occupancy of the deep traps in the bulk of the substrate. For a low N_{eff}, the space charge region at the interface between the substrate and the active layer will be very diffuse and backgating will be minimal.

Calculations of the magnitude of backgating as a function of the substrate compensation using this model are discussed below. In these calculations, the change of the drain current ΔI for a -2-V and -4-V bias applied to the substrate side of the MESFET channel is determined. The relationship between the depletion layer width at the substrate-channel region interface and the excess charge N_{eff} in the space charge region is derived using the standard application of Poisson's equation and the neutrality condition which in this case is

$$\int_0^d N_D(x)\,dx = N_{\text{eff}}W \quad (4)$$

where d is the depletion width on the channel-region side ($N_D(x)$ is the charge distribution in this region) and W is the depletion width on the substrate side (N_{eff} is the constant negative charge in this region). Using these conditions, the general form for the voltage appearing across the

space charge region is derived to be

$$V=\frac{q}{\epsilon}\left\{d\int_0^d N_D(x)\,dx-\int_0^d\left(\int_0^x N_D(x)\,dx\right)dx + \frac{1}{2N_{\text{eff}}}\left(\int_0^d N_D(x)\,dx\right)^2\right\} \quad (5)$$

where V is the sum of the built-in voltage and the applied backgate bias. In these calculations, it is assumed that the active region donor concentration can be represented by

$$N_D(x)=N_D[1-\exp(-x/t)] \quad (6)$$

where N_D and t are determined by a fit to the free-carrier concentration profile used in the experimental devices. This approximation, made as a matter of computational convenience, is a good representation for the recessed gate devices investigated. Using (5) and (6), we obtain

$$V=N_Dq/\epsilon\{d^2/2+t[d\exp(-d/t)+t\exp(-d/t)-t] + N_D/2N_{\text{eff}}[d-t[1-\exp(d/t)]]^2\}. \quad (7)$$

This relationship allows the determination of d for given values of N_D, t, N_{eff}, and V. The value of N_{eff} is given by (3) and the values of N_D and t are given by the fit to the experimental concentration profile in the channel region. Therefore, for different values of V, the depletion depth d in the back-channel region is determined.

The saturated drain current at zero gate bias is calculated using

$$I(d)=\int_d^T qv_sWN_D(x)\,dx \quad (8)$$

where v_s is the saturated velocity, W is the gate width, and T is the total channel region thickness minus the Schottky-gate depletion width. Using the assumed doping profile (6), the general expression for the drain current is

$$I_D=qv_sWN_D\{(T-d)+t[\exp(-T/t)-\exp(-d/t)]\}. \quad (9)$$

Finally, the results of these calculations are shown in Fig. 7 where the drain current with 0, −2-V, and −4-V backgate bias are plotted as a function of N_{eff}. The data shown in Fig. 7 were calculated using the following parameters: $N_D=2.25\times10^{17}$ cm^{-3}, $t=0.1$ μm, $T=0.13$ μm, $W=20$ μm, $v_s=10^7$ cm s^{-1}, and $V_{bi}=0.7$ V.

This figure graphically demonstrates the role of the substrate compensation on the drain current for zero, −2-V, and −4-V backgate bias. For example, if N_{eff} equals 1×10^{16} cm^{-3}, the application of a −2-V backgate bias reduces the drain current by 0.88 mA, 22 percent, and a −4-V backgate bias reduces the drain current by 1.55 mA, 39 percent. If N_{eff} equals 1×10^{15} cm^{-3}, the decrease in the drain current is 0.35 mA, 9 percent, and 0.55 mA, 14 percent, at −2-V and −4-V backgate bias, respectively. The shallow- and deep-level concentrations corresponding to these values of N_{eff} can be determined from (3). For example, if the EL(2) concentration is 1×10^{16} cm^{-3} and the difference in the shallow-level concentration (N_d-N_a) is 5×10^{15} cm^{-3} then a Cr concentration of 1.8×10^{16} cm^{-3} yields N_{eff} equal to 1×10^{16} cm^{-3} and a Cr concentration of 6×10^{15} cm^{-3} yields N_{eff} equal to 1×10^{15} cm^{-3}. Therefore, using these calculations, the magnitude of backgating can be determined if the properties of the substrate and the active region doping concentration profile are known. In general, the backgating effect is minimized if N_{eff} is small.

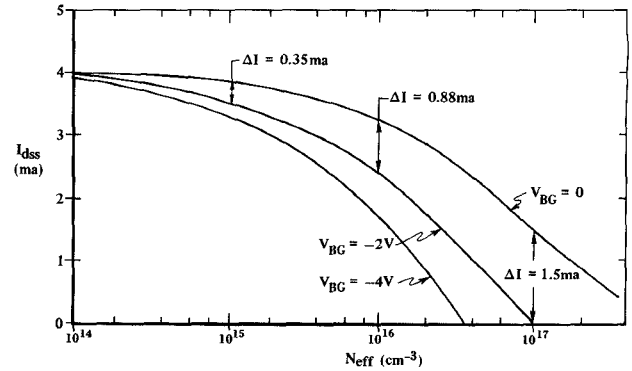

Fig. 7. The calculated dependence of the drain current I_{dss} on the degree of substrate compensation N_{eff} for different backgate bias voltages V_{BG}.

This backgating model has been evaluated in a preliminary experiment in which MESFET test devices were fabricated in low Cr-doped material, approximately 5×10^{15} cm^{-3} Cr concentration. The measured backgating characteristics, represented by the first data point, Cr (shown in Fig. 3), are in qualitative agreement with the model and demonstrate reduced backgating for closely compensated material. The calculations described above assume that the entire backgate voltage is applied at the substrate-channel region interface. A model for the voltage communication between the side-gate and the back-channel region will be developed to permit a more quantitative correlation between the calculated and experimental results. Experiments using proton bombardment isolation to reduce the voltage communication between the side-gate and the back-channel region have demonstrated a decrease in the magnitude of backgating for a given side-gate bias [19].

The model predicts that the use of an n^+ layer, separated from the active region by a buffer layer, would eliminate backgating. In this structure, the excess negative charge N_{eff} in the substrate would produce a narrow space charge region entirely in the n^+ region. Therefore, the space charge will not reach the channel region and no change in the channel width would be produced by a back-gate bias. This postulate, based on the backgating model, will be evaluated experimentally.

V. Conclusions

The results of this experimental investigation indicate that the phenomenon of backgating is the result of an accumulation of excess charge at the substrate-channel region interface. This charge resides on deep traps in the substrate material, either on Cr and EL(2) levels in Cr-doped substrates or on EL(2) levels in high-purity semi-insulating substrates. The deep levels responsible for back-

gating were determined from spectral response and DLTS measurements. Calculations based on this model predict that the magnitude of backgating is dependent on the degree of compensation in the substrate material. Closely compensated substrates have less backgating than substrates with a large excess of deep traps which are unoccupied in the bulk. Preliminary experimental results on lightly Cr-doped material support this model.

Other solutions to the backgate problem include the use of thick buffer layers or n^+ layers as described above. These solutions assure that the space charge region at the semi-insulating to n layer interface does not extend to the MESFET channel region. These solutions and their effect on integrated circuit performance are under investigation.

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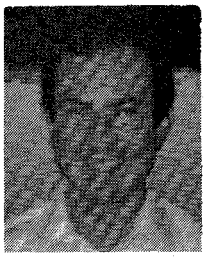

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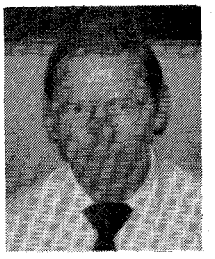

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